# EUROPEAN PATENT APPLICATION

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(54) Synchronisation of digital audio signals.

(57) A digital audio signal which is subject to sample-to-sample jitter is synchronised with local reference pulses (READ) by the use of a read-write buffer memory (12). Timing pulses (80) are associated with the input samples. The input samples are applied through a one-sample latch store (36) to the main memory, and the timing pulses are applied by switches (66,68) either directly or a short delay (38) to the write control input of the main memory. A phase comparator (24; Fig. 3) detects sample-by-sample when the write pulses are near to the read pulses and causes the switches to change state in response thereto, and they retain their changed state until a danger of potential read-write contention is again detected when they revert to their original state.
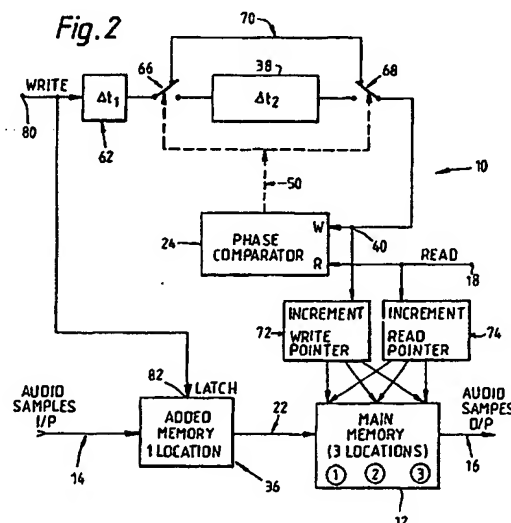
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Fig.2

This invention relates to the reception and synchronisation of digital signals, and particularly digital audio signals.

In large multichannel digital audio systems FIFO (first in, first out) stores are commonly used to delay audio samples for synchronisation purposes. Constraints are placed on the relative timing of the read and write operations for these stores. Such a store has a "busy" output line which is enabled whenever either a write operation or a read operation takes place which inhibits any simultaneous attempt at a read or write operation respectively.

In normal operation write and read operations take place alternately. However, if the write and read operations occur more or less in phase with one another, then a small amount of jitter or timing uncertainty on the received samples may have the effect of momentarily reversing the order in which the write and read operations occur. This will result either in repeated samples or in lost samples, and consequent degradation of the sound quality.

This is illustrated in Figure 1 of the drawings, which shows WRITE and READ operations in four different situations. In case A, the READ and WRITE pulses are widely separated in time. In case B, READ and WRITE are closer than the maximum timing uncertainty, which is represented by the shaded regions. The result of this can be as in case C, where READ and WRITE occur in what is effectively a random order each cycle.

This is thus an example of a situation where an asynchronous input signal subject to sample-to-sample jitter is required to be synchronised with a local reference by the use of a read-write buffer memory.

The invention is defined in the appended claims to which reference should now be made.

A preferred digital signal receiving and synchronising system embodying the invention and designed particularly for use with audio signals is described in more detail below with reference to the drawings. In the preferred system, a digital audio signal which is subject to sample-to-sample jitter is synchronised with local reference pulses by the use of a read-write buffer memory. Timing pulses are associated with the input samples. The input samples are applied through a one-sample latch store to the main memory, and the timing pulses are applied by switches either directly or a short delay to the write control input of the main memory. A phase comparator detects sample-by-sample when the write pulses are near to the read pulses and causes the switches to change state in response thereto, and they retain their changed state until a danger of potential read-write contention is again detected when they revert to their original state.

The invention will be described by way of example with reference to the drawings, in which:

Figure 1 (referred to above) is a timing diagram illustrating the relative timing of WRITE and READ pulses when the WRITE pulses are subject to jitter;

Figure 2 is a block circuit diagram of a preferred digital audio receiver and synchroniser embodying the invention; and

Figure 3 is a block circuit diagram of the phase comparator circuit 24 of Figure 2.

Figure 2 is a block schematic of one embodiment of the invention. The circuit 10 illustrated includes a FIFO store 12 which can contain three input samples and provides a buffer function for the audio samples received at an input 14. The audio signals are received in conjunction with a WRITE timing signal at a terminal 80. The memory 12 provides output samples to an output 16 in response to READ pulses received at a terminal 18 and applied to a read control circuit 74. The output samples may then be applied to a digital to analogue converter for example. The converter requires audio sample data consistently synchronous with the READ pulses.

The write pulses at input 80 are associated with audio samples received at the input 14, and in this case both are derived from the same source, though the write pulses may be produced in other ways. In normal operation, these pulses are used as a latching signal applied to the latching input 82 of an added memory 36, and a short time Δt_1 later after passing through a delay element 62, as write pulses for the main memory 12. Δt_1 is a very short delay equal to the propagation delay of the added memory 36. The output of the added memory 36 is connected directly to the input of the main memory by line 22. Thus, in normal operation, the added memory behaves virtually transparently, adding a small propagation delay to the input of the main memory.

A phase comparator 24 compares the write and read pulses applied to the main memory. If a write pulse approaches too closely to a read pulse, the phase comparator provides a single pulse at its output. This pulse is applied by control line 50 to switches 66,68. These switches allow a relatively long delay element 38 of delay Δt_2 to be admitted into the write signal path. Thus, dependent upon the positions of linked switches 66,68 the write pulses arrive at the write control circuit 72 of the main memory either directly through line 70, or through the delay 38 of value Δt_2. The magnitude Δt_2 of the delay 38 is greater than the overall expected peak-to-peak timing jitter as shown by the shaded area in Figure 1 at B. The added memory 36 contains one location, and therefore requires only a latch signal 82. The output of this

additional memory on line 22 is equal to the latched contents after a short propagation delay.

The system checks read and write signal pulses for every incoming audio sample, and is thus able to follow sample-by-sample timing variations of the type found in digital audio systems (as opposed to slowly drifting variation relative to a fixed reference). Each measurement relates to an individual sample.

Switches 66,68 change state each time a pulse is received from the phase comparator i.e. they operate as toggles. That is, once the delay 38 has been brought into use, further measurements are made using the thus-delayed WRITE pulses, until potential read/write contention is again detected. Then the delay 38 is no longer used. Such an arrangement makes for a much more elegant design and only requires a few memory locations.

When used in a digital audio environment the maximum allowable jitter can be defined for a given level of communication link performance. The phase or timing difference is measured by reference to a high frequency clock, that is a clock which has a frequency much higher than the data rate. This measurement itself introduces an additional jitter component which must also be allowed for in the calculation of delay value Δt_2. If the measured phase difference is greater than the peak jitter possible, then data passes transparently through the additional memory 36 subject to a small delay Δt_1. If the measured phase difference is smaller than the maximum jitter possible, then the data is held in the additional memory for a much longer time Δt_2. After this time it is written to main memory.

The net result is to move the write operation a safe distance in time away from the read operation. This is illustrated at D in Figure 1, where the WRITE pulses are delayed by a fixed amount X greater than the timing uncertainty.

The relative phases of the write and read operations then continue to be monitored by the phase measurement circuit and, if a clash is again detected, the additional store is effectively rendered transparent.

Conveniently the additional memory 36 and the main memory 12 can be constituted by a single 4-sample memory with the additional memory 36 being constituted by the first sample location of the memory.

Figure 3 illustrates a possible circuit for use as the phase comparator 24 to detect instances of potential read/write contention. Read pulses are received at terminal 18 and write pulses at a terminal 40. The read pulses are applied through two delays 42,44 of the same length as delay 38. A gate 46 is opened by the read pulses received at terminal 18 and is closed by the pulses from the

output of delay 44. The write pulses are applied to a similar delay 48 and thence to the gate 46. If a delayed write pulse arrives at the gate when it is open, then the pulse passes through the gate and toggles the switches 66,68.

The circuits illustrated can be implemented in the form of an integrated circuit device and can be incorporated into a digital audio interface in accordance with IEC 958. They have the advantage of providing synchronism in a system where the master clock is not derived from the input pulses and yet provide a very small overall delay to the signal.

Claims

1. A method of receiving a digital signal the samples of which are subject to timing uncertainty and synchronising them with a reference source, comprising the steps of:

    providing a main read-write memory capable of storing at least one sample and having a data input, a data output, a write control input and a read control input;

    selectively in one of two possible modes applying the input samples and also timing pulses related to the input samples to the main memory, namely either apply the timing pulses to the write control input of the main memory and applying the input samples to the data input of the main memory substantially without delay, or applying the timing pulses to the write control input through a timing pulse delay and applying the input samples to the data input through a data sample delay; and

    comparing the timing of successive pulses applied to the write control input and the read control input of the main memory, and, if the pulses approach to within less than a predetermined time interval related to the timing uncertainty of the input signal, changing the mode of application of the timing pulses and input samples to the main memory.

2. A method according to claim 1, in which the digital signal is a digital audio signal.

3. Digital signal receiving and synchronising apparatus for receiving a digital signal the samples of which are subject to timing uncertainty and synchronising them with a reference source, comprising:

    a signal input for receiving the digital signal;

    means for providing timing pulses corresponding to the receipt of samples at the signal input;

    a terminal for receiving reference pulses with respect to which the digital signal is to be

synchronised;

a main read-write memory means capable of storing at least one sample and having a data input, a data output constituting the output of the apparatus, a write control input, and a read control input connected to the said terminal to receive reference pulses;

additional memory means capable of storing one sample,

a timing pulse delay;

selector means having a control input and which in a first condition applies pulses from the timing pulse providing means to the write control means of the main memory means and applies the signal input to the data input of the main memory means substantially without delay in the additional memory means, and in a second condition connects the timing pulse providing means through the timing pulse delay to the write control means of the main memory means and connects the signal input through the additional memory means to the data input of the main memory means; and

timing comparison means connected to receive successive pulses applied to the write control input and to the read control input of the main memory means for comparing the timing thereof and if the pulses approach to within less than a predetermined time interval related to the timing uncertainty of the input signal applying a control signal to the control input of the selector means to change the condition thereof from its first condition to its second condition, or vice versa as the case may be.

4. Apparatus according to claim 3, in which the timing pulse delay is at least equal to the said predetermined time interval.

5. Apparatus according to claim 3 or 4, in which in the first condition of the selector means the additional memory means is effectively rendered transparent to the input signal.

6. Apparatus according to any of claims 3 to 5, in which the main memory means is capable of holding up to three samples.

7. Apparatus according to any of claims 3 to 6, in which the main memory means and the additional memory means are constituted by a single memory.

8. Apparatus according to any of claims 3 to 7, in which the timing comparison means comprises a first timing comparison delay for delaying reference pulses received at the said terminal by an amount substantially twice the delay of the said timing pulse delay; a second timing comparison delay for delaying the pulses applied to the write control input of the main memory means by an amount substantially equal to the delay of the timing pulse delay; and gate means having an input connected to receive the delayed write pulses from the second timing comparison delay and an output constituting the output of the timing comparison means, and having an OPEN input connected to the said terminal to receive the reference pulses to open the gate means and a CLOSE input connected to the output of the first timing comparison delay to close the gate means in response to the delayed reference pulses.

9. The use, to receive a digital audio signal the samples of which are subject to timing uncertainty and to synchronise them with a reference source, of digital signal receiving and synchronising apparatus in accordance with any preceding claim.

Fig.1

Fig.2

Fig.3